

# LH53B16P00

**CMOS 16M (2M × 8/1M × 16) Mask-Programmable ROM With Page Mode**

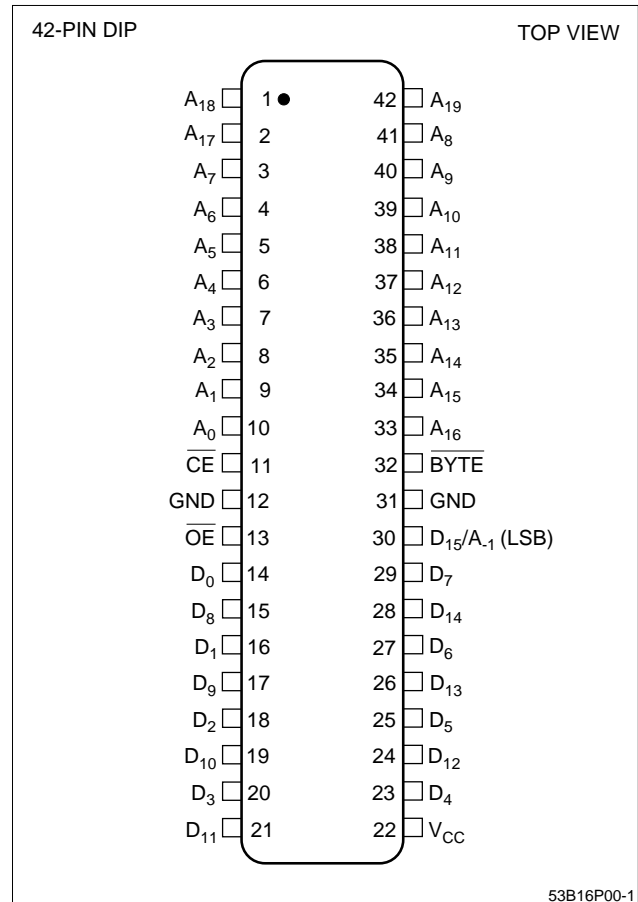
## FEATURES

- 2,097,152 words × 8 bit organization (Byte mode)
- 1,048,576 words × 16 bit organization (Word mode)
- Access time: 120 ns (MAX.)  
Page mode: 50 ns (MAX.)
- Addressable page: 4 words or 8 bytes
- Power consumption:  
Operating: 550 mW (MAX.)  
Standby: 1650 μW (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:  
42-pin, 600-mil DIP  
44-pin, 600-mil SOP

## DESCRIPTION

The LH53B16P00 is a 16M-bit mask-programmable ROM organized as 2,097,152 × 8 bits (Byte mode) or 1,048,576 × 16 bits (Word mode) with page mode operation. It is fabricated using silicon-gate CMOS process technology.

## PIN CONNECTIONS



**Figure 1. Pin Connections for DIP Package**

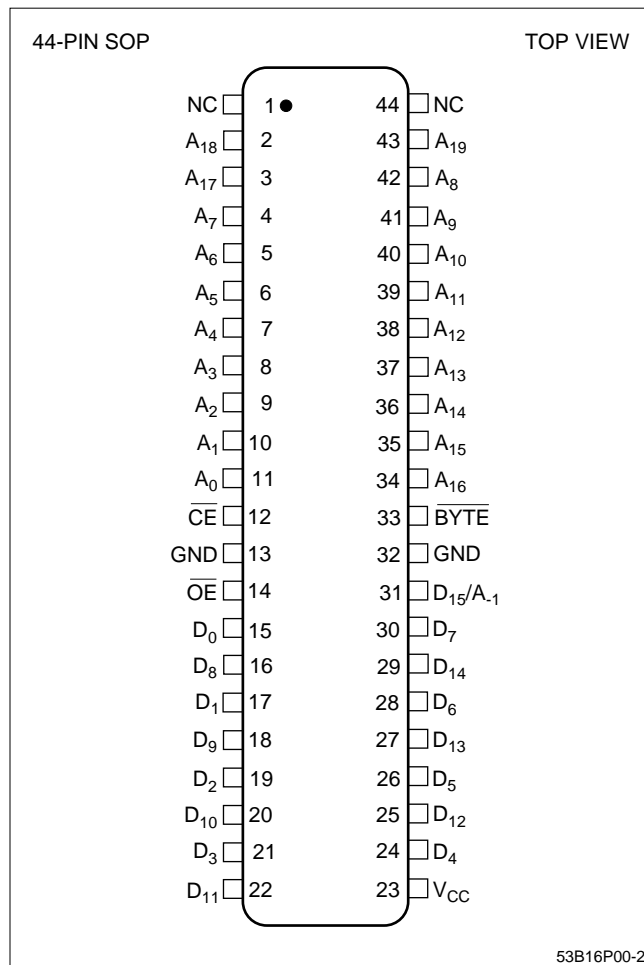


Figure 2. Pin Connections for SOP Package

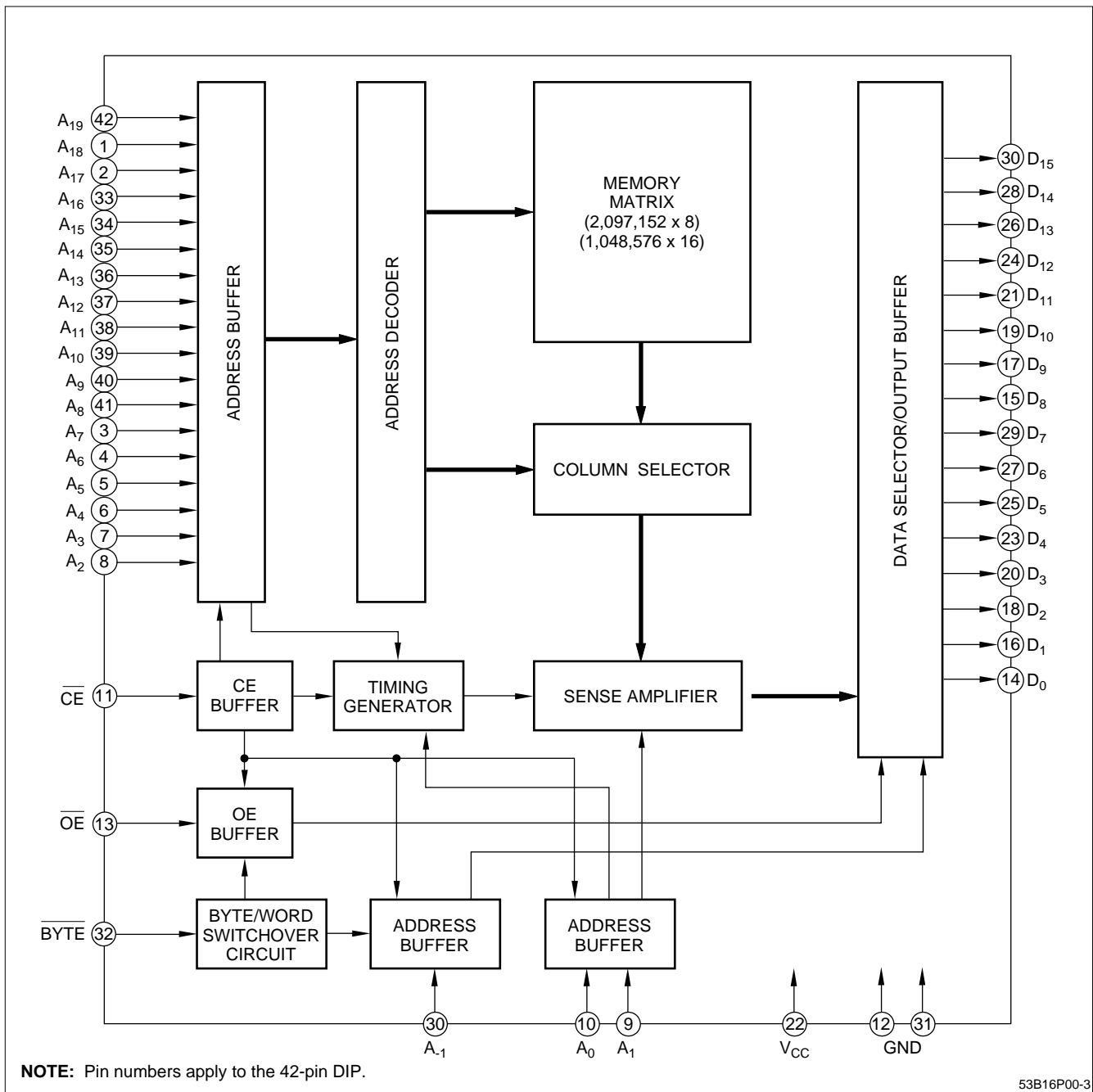


Figure 3. LH53B16P00 Block Diagram

**PIN DESCRIPTION**

SIGNAL	PIN NAME	NOTE
A <sub>1</sub> – A <sub>1</sub>	Address input (page mode operation)	1
A <sub>2</sub> – A <sub>19</sub>	Address input	
D <sub>0</sub> – D <sub>15</sub>	Data output	1
BYTE	Byte/word mode switch	1

SIGNAL	PIN NAME	NOTE
CE	Chip enable input	
OE	Output enable input	
V <sub>CC</sub>	Power supply (+5 V)	
GND	Ground	

**NOTE:**

- The D<sub>15</sub>/A<sub>1</sub> pin becomes LSB address input (A<sub>1</sub>) when the BYTE pin is set to be LOW in byte mode, and data output (D<sub>15</sub>) when set to be HIGH in word mode.

## TRUTH TABLE

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{BYTE}}$	A <sub>-1</sub> (D <sub>15</sub> )	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
				D <sub>0</sub> – D <sub>7</sub>	D <sub>8</sub> – D <sub>15</sub>	LSB	MSB	
H	X	X	X	High-Z	High-Z	–	–	Standby (I <sub>SB</sub> )
L	H	X	X	High-Z	High-Z	–	–	Operating (I <sub>CC</sub> )
L	L	H	–	D <sub>0</sub> – D <sub>7</sub>	D <sub>8</sub> – D <sub>15</sub>	A <sub>0</sub>	A <sub>19</sub>	Operating (I <sub>CC</sub> )
L	L	L	L	D <sub>0</sub> – D <sub>7</sub>	High-Z	A <sub>-1</sub>	A <sub>19</sub>	Operating (I <sub>CC</sub> )
L	L	L	H	D <sub>8</sub> – D <sub>15</sub>	High-Z	A <sub>-1</sub>	A <sub>19</sub>	Operating (I <sub>CC</sub> )

## NOTE:

X = H or L

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V <sub>CC</sub>	–0.3 to +7.0	V
Input voltage	V <sub>IN</sub>	–0.3 to V <sub>CC</sub> + 0.3	V
Output voltage	V <sub>OUT</sub>	–0.3 to V <sub>CC</sub> + 0.3	V
Operating temperature	T <sub>opr</sub>	0 to +70	°C
Storage temperature	T <sub>stg</sub>	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = 0°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V

DC CHARACTERISTICS (V<sub>CC</sub> = 5 V ±10%, T<sub>A</sub> = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V <sub>IL</sub>		–0.3		0.8	V	
Input 'High' voltage	V <sub>IH</sub>		2.2		V <sub>CC</sub> + 0.3	V	
Output 'Low' voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.0 mA			0.4	V	
Output 'High' voltage	V <sub>OH</sub>	I <sub>OH</sub> = –400 μA	2.4			V	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 V to V <sub>CC</sub>			10	μA	
Output leakage current	I <sub>LO</sub>	V <sub>OUT</sub> = 0 V to V <sub>CC</sub>			10	μA	1
Operating current	I <sub>CC1</sub>	t <sub>RC</sub> = 150 ns			100	mA	2
	I <sub>CC2</sub>	t <sub>RC</sub> = 1 μs			80	mA	2
Standby current	I <sub>SB1</sub>	$\overline{\text{CE}} = V_{IH}$			2	mA	
	I <sub>SB2</sub>	$\overline{\text{CE}} = V_{CC} - 0.2 \text{ V}$			300	μA	
Input capacitance	C <sub>IN</sub>	f = 1 MHz			10	pF	
Output capacitance	C <sub>OUT</sub>	T <sub>A</sub> = 25°C			10	pF	

## NOTES:

- $\overline{\text{CE}}/\overline{\text{OE}} = V_{IH}$
- V<sub>IN</sub> = V<sub>IH</sub> or V<sub>IL</sub>,  $\overline{\text{CE}} = V_{IL}$ , outputs open

**AC CHARACTERISTICS ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	$t_{RC}$	120			ns	
Address access time	$t_{AA}$			120	ns	
Chip enable access time	$t_{ACE}$			120	ns	
Page address access time	$t_{APA}$			50	ns	
Output enable delay time	$t_{OE}$			50	ns	
Output hold time	$t_{OH}$	5			ns	
CE to output in High-Z	$t_{CHZ}$			50	ns	1
OE to output in High-Z	$t_{OHZ}$			40	ns	1
CE to output in Low-Z	$t_{CLZ}$	5			ns	
OE to output in Low-Z	$t_{OLZ}$	5			ns	

**NOTE:**

1. This is the time required for the outputs to become high-impedance.

**AC TEST CONDITIONS**

PARAMETER	RATING
Input voltage amplitude	0.4 V to 2.6 V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1TTL + 100 pF

**CAUTION**

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the  $V_{CC}$  pin and the GND pin.

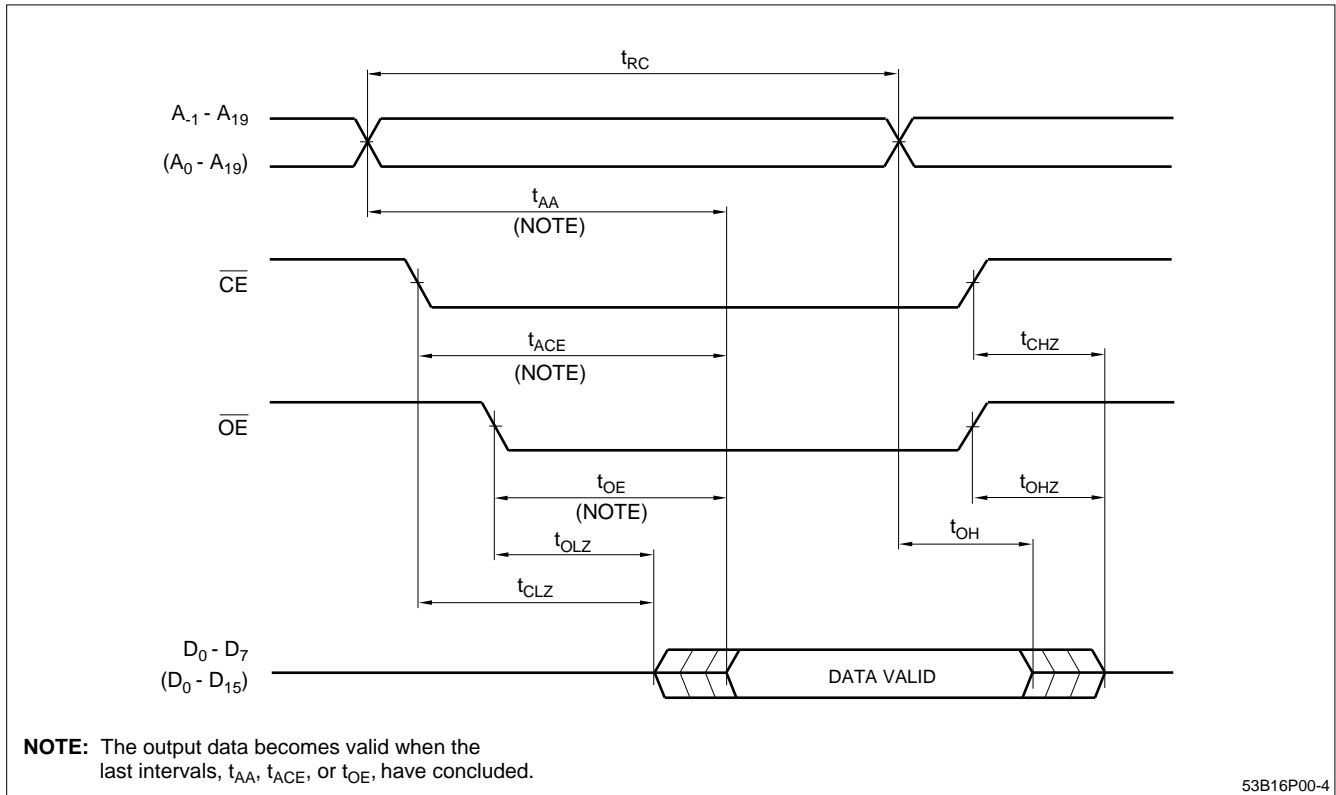


Figure 4. Read Cycle

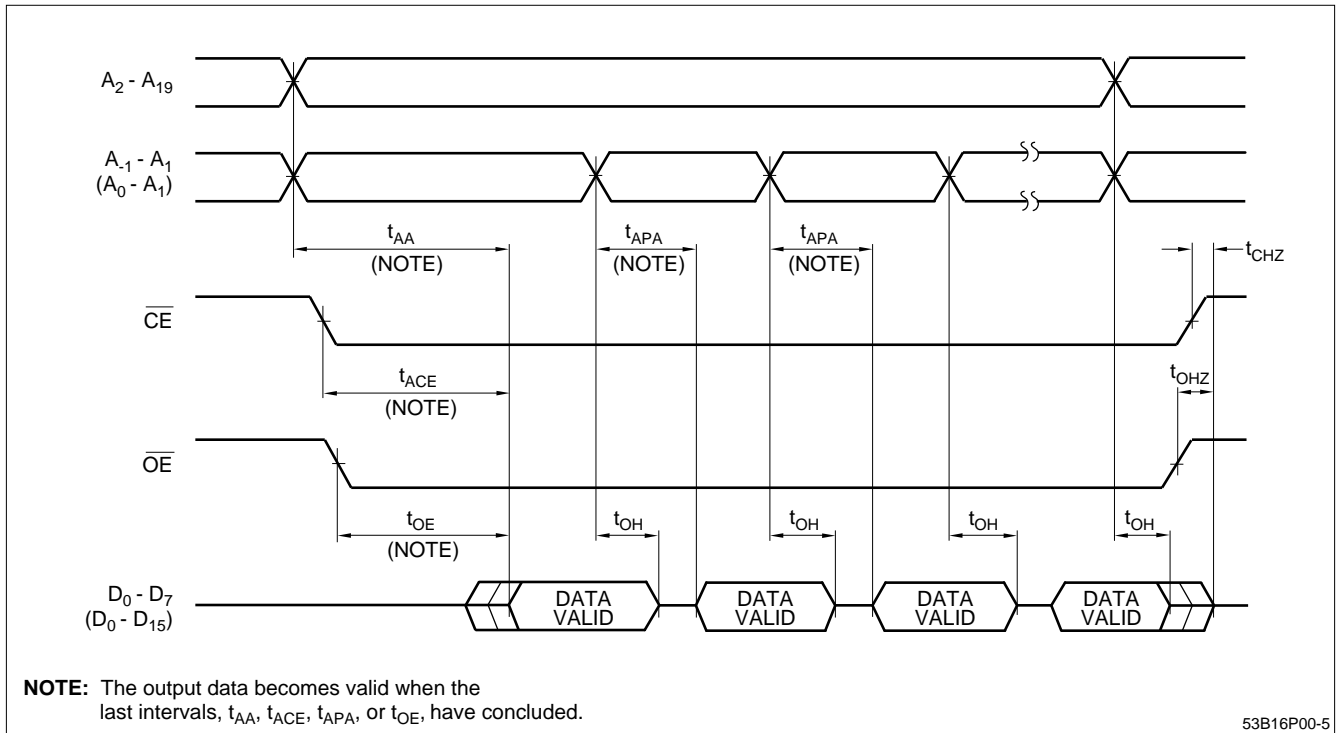
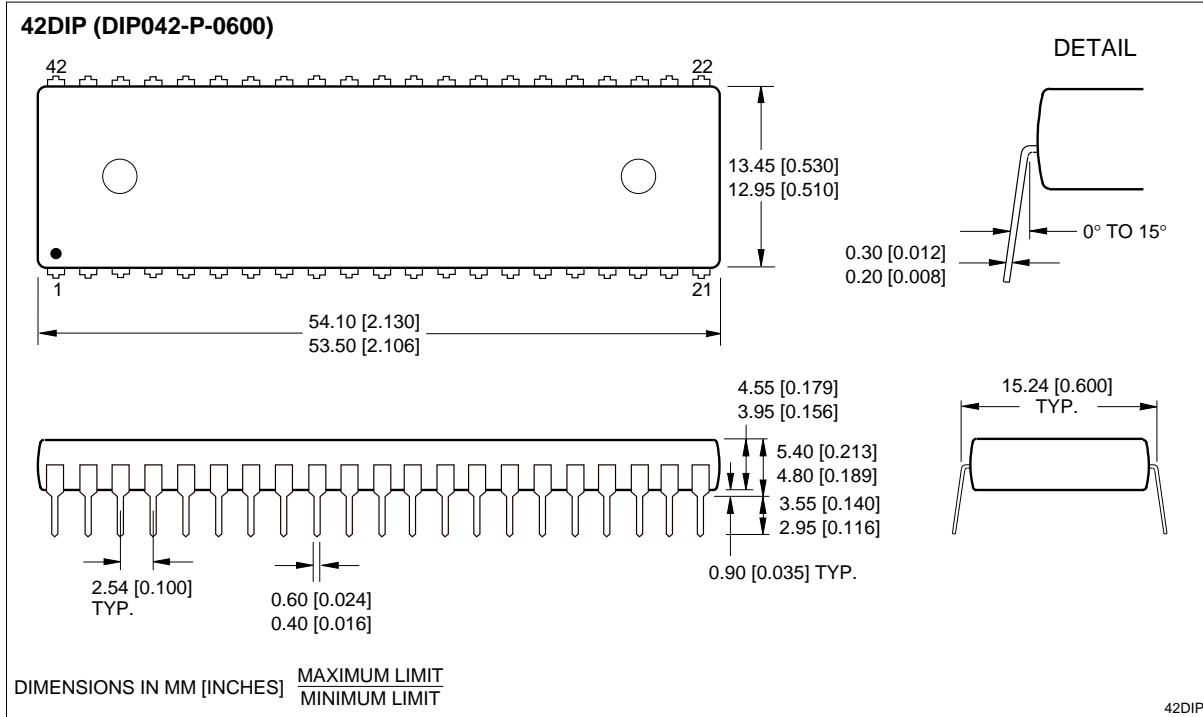
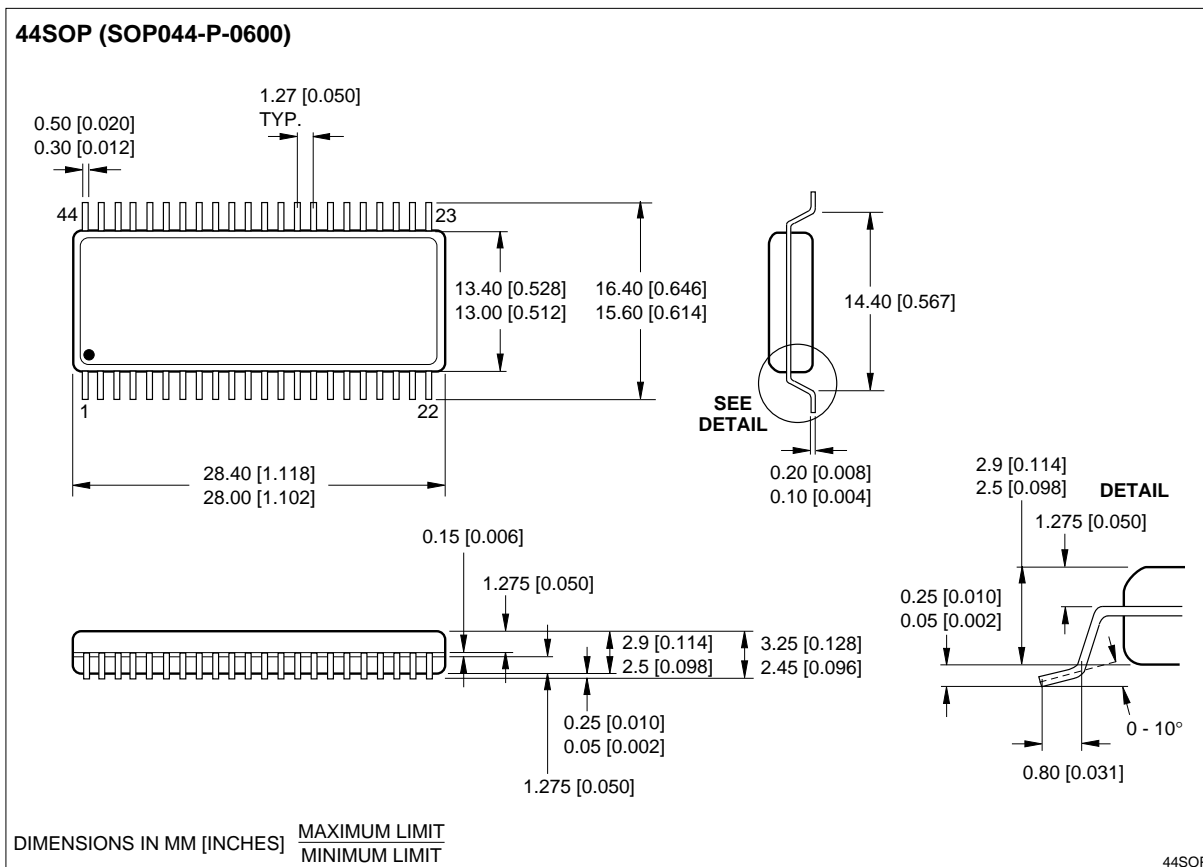


Figure 5. Page Mode Read Cycle

PACKAGE DIAGRAMS

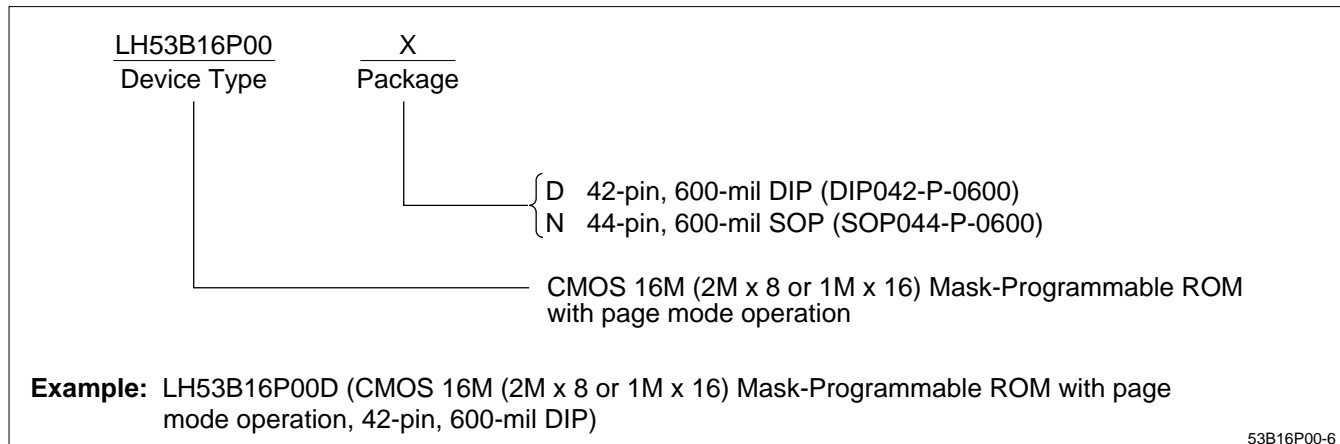


42-pin, 600-mil DIP



44-pin, 600-mil SOP

## ORDERING INFORMATION



53B16P00-6